Objected to Claims 12-17 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Claims 12-17 stand allowable.

Claim 11 stand rejected under 35 U.S.C. 102(b) as being anticipated by Yassa et al (US 4,862,098). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claim 11 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 11 requires and positively recites, a phase-locked loop system comprising: "a digitally-controlled oscillator **responsive to an oscillator tuning word (OTW)** to generate an oscillator clock", "**a direct modulator operational in response to a modulating data signal and a phase error to generate the OTW**" and "a phase-locked loop (PLL) operational in response to **a channel selection signal** and the modulating data signal to generate the phase error".

In contrast, the circuits that Yassa discloses are demodulators of a modulated-carrier signal. As an example, in Figure 4 (that the examiner brought up), the modulated signal from source 31 is being subtracted by the [illegible]

error signal is then downconverted by the carrier multiplication (multipliers 14 and 34) and then filtered out by the accumulators (22, 16 and 42, 36). The output is the demodulated signal.

Comparing Yassa's circuit with the present invention the following differences are obviously noted:

1. Yassa's circuit is a demodulator, the present invention discloses a modulator – a completely reversed process. Yassa's circuit produces a demodulated (downconverted) signal, the present invention produces modulated (upconverted) signal;

2. Yassa's circuit does not have a modulating signal as in the present invention. Source 31 is the modulated signal. The difference is that the modulating signal is at baseband, whereas the modulated signal is at higher-frequency.

3. In the present invention, the DCO is a frequency-modulated carrier source ("a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock" in Clam 11). DCO 301 in Yassa is only a carrier signal source.

4. Claim 11 contains "channel selection", which does not exist in Yassa patent.

5. Yassa's patent is a demodulator that constantly tracks the adapting coefficients using a least mean square (LMS) fit. It is not a phase-locked loop, as in the present invention. There is, however, a DCO feedback mechanism in Yassa, but its purpose is to bring the average (filtered) value of the complex demodulated output to zero. Neither that is a phase-locked loop.

In light of the comments above, it is fairly clear that Claim 11 is not anticipated by the Yassa reference. Accordingly, the 35 U.S.C. 102(b) rejection of Claim 11 is overcome.

New Claims 22-24 stand allowable as depending from allowable claims and including further limitation not taught or suggested by the references of record. More particularly, Claims 22-24 further define the term "phase error" to be --filtered phase error--.

New Claim 25 is allowable since it is a redraft of allowed Claim 18 without the unduly limiting actual equation for the DCO gain.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Claims 1-10 and 18-21 stand allowed and should continue to stand allowed in light of the minor amendments made to Claims 1, 2, 4 and 6. Objected to Claims 12-17 stand allowable since Claims 12-17 have been rewritten in independent forming including all of the limitations of the base claim and any intervening claim. Claim 11 and new Claims 22-25 stand allowable over the cited art and the application is in allowable form. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

Ronald O. Neerings
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4417

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS – (marked-up copy):

1. (amended) A digital phase-domain phase-locked loop circuit comprising:

a digitally-controlled oscillator (DCO);

a gain element feeding the DCO and operational to compensate for DCO gain in response to a loop gain alpha multiplier signal;

an oscillator phase accumulator operational to accumulate DCO generated clock edges;

a reference phase accumulator operational to accumulate a frequency division ration command and a modulating data signal and to generate an accumulated frequency control word (FCW) therefrom;

a phase detector operational to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a [filtered] phase error in response thereto;

a loop gain alpha multiplier element operational to generate the loop gain alpha multiplier signal in response to a filtered direct modulator output signal; and

a direct modulator operational in response to the modulating data signal and the filtered phase error to generate the filtered direct modulator output signal.

2. (amended) The digital phase-domain phase-locked loop circuit according to claim 1 wherein the direct modulator comprises:

a loop gain alpha inverse multiplier element operational to generate a signal in response to the modulating data signal; and

a combinational element feeding the loop gain alpha multiplier element in response to the signal generated by the loop gain alpha inverse multiplier element and further in response to the [filtered] phase error.

[illegible] detector to generate the [filtered] phase error.

6. (amended) A digital phase-domain phase-locked loop circuit comprising:

a digitally-controlled oscillator (DCO);

a gain element feeding the DCO and operational to compensate for DCO gain in response to a direct modulator output signal;

an oscillator phase accumulator operational to accumulate DCO generated clock edges;

a reference phase accumulator operational to accumulate a frequency division ratio command and a modulating data signal and to generate an accumulated frequency control word (FCW) therefrom;

a phase detector operation to compare the accumulated FCW and the accumulated DCO generated clock edges and generate a [filtered] phase error in response thereto;

a loop gain alpha multiplier element operational to generate a loop gain alpha multiplier signal in response to the [filtered] phase error; and

a direct modulator operational in response to the modulating data signal and the alpha multiplier signal to generate the direct modulator output signal.

9. (amended) The digital phase-domain phase-locked loop circuit according to claim 6 further comprising an all-pass filter operational to pass said phase error generated via the phase detector to generate [the] a filtered phase error.

11. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a [filtered] phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the [filtered] phase error.

12. (amended) A phase-locked loop system comprising:

[oscillator clock.] The phase-locked loop system according to claim [1] wherein the digitally-

controlled oscillator comprising[es] a voltage controlled oscillator; and a digital-to-analog converter operational to generate an oscillator tuning voltage in response to the OTW;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

13. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW, said [The phase-locked loop system according to claim 11 wherein the] direct modulator comprising[es] a combinational element feeding the digitally controlled oscillator such that an oscillator gain can be compensated to substantially remove its effects on loop behavior[.]; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error.

14. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW;

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error; and

[The phase-locked loop system according to claim 11 further comprising] a direct modulation switch element operational to selectively attenuate a feed-forward path associated with the PLL.

17. (amended) A phase-locked loop system comprising:

a digitally-controlled oscillator responsive to an oscillator tuning word (OTW) to generate an oscillator clock;

a direct modulator operational in response to a modulating data signal and a filtered phase error to generate the OTW; and

a phase-locked loop (PLL) operational in response to a channel selection signal and the modulating data signal to generate the filtered phase error, said [The phase-locked loop system according to claim 11 wherein] PLL comprising[es] a phase detector feeding an all-pass filter, wherein the phase detector is responsive to the channel selection signal and the modulating data signal to generate said phase error, and wherein the all-pass filter is operational to pass the phase error to generate [the] a filtered phase error.

Please add the following new claims:

22. The digital phase-domain phase-locked loop circuit according to claim 1 wherein said phase error is a filtered phase error.

23. The digital phase-domain phase-locked loop circuit according to claim 6 wherein said phase error is a filtered phase error.

24. The phase-locked loop system according to claim 11 wherein said phase error is a filtered phase error.

25. A method of operating a digital phase-locked loop (PLL) comprising the steps of:

providing a phase-locked loop including a digitally-controlled oscillator (DCO) having a gain K_{DCO}, and a phase detector, wherein the DCO is responsive to an oscillator tuning word (OTW) to generate a DCO output clock having a frequency fv, and further wherein the phase detector is responsive to a channel selection signal, a modulating data signal and the output clock to

providing a direct modulator operational in response to the phase error and the modulating data signal to generate the OTW;

observing an accumulated phase $\Delta\emptyset$ in the phase error in response to a given change Δx in the OTW; and

estimating the DCO gain such that a DCO gain can be compensated to substantially remove its effects on loop behavior.